CV - Björn Berglöf

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Summary

Wide experience as chip/electronics designer: Asic / Fpga / Sw / Embedded.

Skills: Technical lead, good verbal/visual/writing communicator, creative and responsible. SystemVerilog/VHDL/Verilog.

Roles: design, system, methodology, trouble shooter, prototyping.

Applications: telecom, Tbps ethernet switching, fighter aircraft, mobile phones, video servers.

Ten year as **self-employed** consultant.

Patents and many patent-worthy designs.

Experience

2016 - present **Lead designer ASIC/FPGA at yDesign**
1000+ MGate asic designs in TSMC16/6nm for high bandwidth ethernet switch/router chips. Responsible for design of switch fabric control. Architecture and design of a pipelined SRAM handler for high rate, multiple ALU, statistical RmW. Created patent level algorithms and design for traffic shaping (high speed arithmetic functions). System and RTL design of hierarchical cpu control structures including dma, event and interrupts. Intricate design for measuring time and latency with 50ps resolution. Various designs involving: BISTs/Test vector routing/Clock synthesis/Chip top level routing/PVT measurements/etc

2011 - 2015 **Senior Asic/Fpga/Sw designer at Marvell.**
Several block designs in TSMC 28nm asics for **200 Gbps ethernet**, including arithmetics, caches and ring-bus structures at very high rates. **Prototyping** using top-end Xilinx FPGAs, enabling hardware and software co-verification before the asic is manufactured. Defining boot sequences, embedded cores and pushing sw/hw-performance.

2006 - 2010 **Senior Fpga Designer at Edgeware**
Designing a **20 Gbps Video-on-demand server**. Several Altera FPGA designs including AES and MD5 crypto, BCH error-correcting-coding, packet classification, multi-channel DMA, metering/shaping of traffic as well as various high-speed interfaces and BIST's. Designing drivers, apps and debug routines in C/Linux.

2002 - 2006 **Senior Asic Designer at Xelerated**
Designing **40 Gbps network processor** (100Mgate+) Responsible for generic DDR-SRAM/FCRAM/RLDRAM/NSE programmable interfaces, handling i/o at 530Mbps/pin. Also designed co-processor in Xilinx FPGA handling high performance shaping and metering.

1993 - 2002 **Own company Mr Bear AB (independent consultant).**

Contract with Ericsson Telecom in Älvsjö, Stockholm 2001-2002.
Designing a **voice processing ASIC** for the AXD301 high performance ATM switch. Designing high performance arithmetic blocks. Used Celaro hardware acclerator for verification.

Contract with Saab Avionics, in Kista, Stockholm 1997-2001.
Designing a graphics processor ASIC for the **Gripen fighter jet**. Tool support and contacts with vendor. Several Altera CPLD/FPGA designs for video processing as well as C++ code in embedded VxWorks environment. Supervising several projects as senior designer as well as giving giving courses and lectures**.**

Contract with Ericsson Communication Systems, Lund 1996-1997.
Asics for **GSM and AMPS mobile phones**. Low voltage and low power design, using VLSI 0.5u and 0.35u asic technology (400+ kgates). Responsible for deep-submicron design flow, and handled libraries and contacts with vendor. Synopsys tool support. Using VHDL and several Mentor Graphics tools.

Contract with Ericsson Telecom, Stockholm 1993-1995.
Designing **SDH telecom equipment** using Motorola 0.5u asic technology (300+ kgates), in Verilog and Synopsys environment. Several designs including: JTAG logic, CPU i/f, High Speed block. Responsible for generating functional test vectors and ATPG vectors.

1988 - 1993 **Consulting Analog/Asic/SW designer at ÅF-Industriteknik, Stockholm.**
Four Texas Instruments asics. Modem designs for laptops (analog design/real-time assembly programming). Parking meters (battery chagers/power supply).

1986 - 1988 **Lecturer at University of Zambia (Africa)**
Giving course: 'Communication Theory and Systems' for final year telecom. students. Supervising BA students electronics projects.

Education

Master of Science in Electrical Engineering
Royal Institute of Technology, Stockholm 1986.
Technician degree 1978**.**

Personal

Outgoing, creative and responsible.
Fluent in English, some German.
Forty years as scuba diver, one star Instructor level.
Married.
Enjoying excellent health.
References available at request.